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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	New- 10 / 827 380
Sheet	1	of	1	Filing Date	Concurrently Herewith
				First Named Inventor	Alon Regev
				Prior Art Unit	2818
				Prior Examiner Name	L. Tran
				Attorney Docket Number	M4065.0579/P579-A

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
UET	AA	6,101,115	08/2000	Ross	
UET	AB	6,240,001 B1	05/2001	Ross	
UET	AC	6,349,049 B1	02/2002	Schoy	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
UET	AD	"Half-Vdd Bit-Line Sensing Scheme in CMOS DRAM's," Nicky Chau-Chun Lu et al., IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984, pp. 451-454			
UET	AE	"A 256M DRAM with Simplified Register Control for Low Power Self Refresh and Rapid Burn-in," Seung-Moon Yoo et al., 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp. 85 and 86			
UET	AF	"Automatic Voltage-Swing Reduction (AVR) Scheme for Ultra Low Power DRAMs," Masaki Tsukude et al., 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp. 87 and 88			
UET	AG	"A 250mV Bit-Line Swing Scheme for a 1V 4Gb DRAM," T. Inaba et al., 1995 Symposium on VLSI Circuits Digest of Technical Papers, pp. 99 and 100			

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